G.723.1

DSP-BASED SPEECH COMPRESSION CODER

Analog Devices' G.723.1 speech compression algorithm, running on a high-performance 33 MIPS Digital Signal Processor (DSP) compresses the speech or any other audio signal component of multimedia software or other audio. This speech coder chipset features multiple bit rates, acoustic echo cancellation and software code which conforms to the ITU H.324 standards family.

The speech coder chipset features two bit rates: 6.3 Kbps and 5.3 Kbps. The higher bit rate offers better quality, while the lower bit rate provides system designers with additional flexibility. Both the encoder and decoder operate at either bit rate to enable switching between the two rates at any frame boundary. An option for variable rate operation enables discontinuous transmission and noise fill during non-speech intervals.

The G.723.1 chipset includes the ADSST-G723-xxxx, a 33-MIPS Digital Signal Processor. The G.723.1 software code requires 20 MIPS, 8.2 KWords PM RAM and 12 KWords DM RAM of the DSP. A demonstration featuring the G.723.1 compression algorithm with or without acoustic echo cancellation is available to run on an Analog Devices EZ-LITE development board.

HIGHLIGHTS

- **Variable Bit Rates: 5.3 Kbps and 6.3 Kbps (Low Bit Rate Enhances Flexibility; High Bit Rate Improves Quality)**

- **High Bit Rate Coder Excitation Signal: MP-MLQ**

- **Low Bit Rate Coder Excitation Signal: ACELP**

- **Discontinuous Transmission And Noise Fill During Non-Speech Intervals**

- **Optimizer Represented In Speech**

- **Encodes Speech Using Linear Analysis-By-Synthesis Coding**

- **Frame Size: 30 msec**

- **Delay Time: 7.5 msec**

The G.723.1 algorithm has been optimized to compress the highest quality speech at the above bit rates with a limited amount of complexity. It encodes speech or other audio signals in frames using linear predictive analysis-by-synthesis coding. The excitation signal for the high rate coder is Multipulse Maximum Likelihood Quantization (MP-MLQ) and for the low rate coder is Algebraic Codebook Excited Linear Prediction (ACELP). The frame size is 30 msec and there is an additional look-ahead of 7.5 msec, resulting in a total algorithmic delay of 37.5 msec. All additional delays in this coder are caused by processing delays of the implementation, transmission delays in the communication link and buffering delays of the multiplexing protocol.